Sole Inventor

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Charissa D. Wheeler

APPLICATION FOR UNITED STATES LETTERS PATENT

S P E C I F I C A T I O N

TO ALL WHOM IT MAY CONCERN:

Be it known that I, **Cheolsoo Park**, a citizen of Republic of Korea, residing at 891-10 Daechi-dong, Gangnam, Seoul, Korea have invented a new and useful **METHOD FOR FORMING METAL LINES IN A SEMICONDUCTOR DEVICE**, of which the following is a specification.

METHOD FOR FORMING METAL LINES IN A SEMICONDUCTOR DEVICE

FIELD OF THE DISCLOSURE

[0001] The present disclosure relates generally to semiconductor devices and, more particularly, to a method for forming metal lines in a semiconductor device.

BACKGROUND

[0002] In general, as semiconductor devices become more highly integrated, the importance of metal lines increases. Specifically, in a logic design technique as well as a memory design technique, the use of a back end of line ("BEOL") process becomes greater than that of a front end of line ("FEOL") process. This trend has caused a decrease in the operating speeds of semiconductor devices due to increases in resistance and parasitic capacitance upon formation of the metal lines.

[0003] For example, U.S. Pat. No. 6,448,649 discloses a method of forming plugs of two layers by deposition of a material for the plugs into holes and U.S. Pat. No. 6,130,102 discloses a method of forming plug of a dual damascene type to prevent a leakage current in a capacitor. However, such conventional methods cause structural problems and result in a high manufacturing cost of the semiconductor device.

BRIEF DESCRIPTION OF THE DRAWINGS

[0004] Figs. Figs. 1A to 1F illustrate cross sectional views sequentially showing an example process of forming metal lines in a semiconductor device.

DETAILED DESCRIPTION

[0005] As described in greater detail below, an example method for forming metal lines in a semiconductor device, includes forming first metal lines and a first insulation layer on the first metal lines, etching the first insulation layer until the first metal lines are exposed, depositing a conductive material into the etched portion

of the first insulation layer to form contact plugs, forming a second insulation layer on the resultant structure, etching the second insulation layer to expose the contact plugs, depositing a material for cores into the etched portions of the second insulation layer to form the cores. In addition, the example method may further include selectively removing the second insulation layer to expose the cores, and depositing a second metal lines on both sides of the cores to branch current to both sides of the cores.

[0006] Referring to Fig. 1A, first metal lines 10 are formed on a semiconductor substrate and a first insulation layer 12 is formed thereon. The first insulation layer 12 is then planarized. A first photoresist pattern 14 for forming contact plugs is formed on the first insulation layer 12 and the first insulation layer 12 is etched by a dry etching process to expose the first metal lines 10.

[0007] As shown in Fig. 1B, after the first photoresist pattern 14 is removed, a conductive material is deposited into the etched portion of the first insulation layer 12 to form the contact plugs 16.

[0008] Subsequently, referring to Fig. 1C, an etch-stop nitride layer 18 and a second insulation layer 20 are deposited on the resultant structure, sequentially. A second photoresist pattern 22 for forming cores is then formed on the second insulation layer 20. The second insulation layer 20 and the etch-stop nitride layer 18 are in turn etched using the second photoresist pattern 22 as a mask, thereby exposing the top surface of the contact plugs 16.

[0009] Referring to Fig. 1D, the second photoresist pattern 22 is removed and a material for the cores 24 is deposited into the etched portions of the second insulation layer 20 to form the cores 24. The material for the cores 24 is preferably TaN or TiN.

[0010] As shown in Fig. 1E, the cores 24 are exposed by selectively dry etching the second insulation layer 20, wherein the second insulation layer 20 is not entirely removed and remains with a small thickness.

[0011] Fig. 1F provides a cross sectional view showing a state after second metal lines 26 are formed on the exposed cores 24 by a blanket etchback process. Specifically, the second metal lines 26 are formed on both sides of the cores 24 by the blanket etchback process, so that current is branched to the both sides of the cores 24. Further, by controlling a height of the cores, a resistance of the metal lines may be decreased.

[0012] With the example apparatus and methods described herein, an electromigration ("EM") characteristic of the metal lines is improved and a manufacturing cost of the semiconductor device is decreased.

[0013] Although certain methods and apparatus have been described herein, the scope of coverage of this patent is not limited thereto. To the contrary, this patent covers all embodiments fairly falling within the scope of the appended claims either literally or under the doctrine of equivalents.